**ELEC2800 PSB**

**COURSE DESCRIPTION**
This is a bridging course, designed to help students familiarise with the basic circuit theory, digital design and low-level programming. These materials are fundamental to most Electrical Engineering, Telecommunications and Mechatronics courses. The course consists of two parts.

- **Part A: Electrical Circuits.** This part covers DC circuit analysis, AC circuit analysis, 3-phase systems, frequency response, resonant circuits, filters and operating amplifiers. It contains 30 hours of lectures and tutorials, 2 one-hour quizzes and 2 three-hour labs.

- **Part B: Digital Design Techniques.** This part includes:
  - Digital design: programmable logic devices, VHDL basics and VHDL design in combinational logic, sequential logic, and state machines;
  - Microprocessor systems: microprocessor architecture and buses, assembly programming language, memory, interrupts, and peripherals.

  It contains 26 hours of lectures and tutorials, a one-hour quiz, and four 2.5-hour labs.

**LECTURING STAFF**
Part A will be taught by Professor Minyue Fu. Minyue can be contacted by email (minyue.fu@newcastle.edu.au) or by phone 61-2-4921773.

Part B will be taught by Dr. Abbas Kouzani. Abbas can be contacted by email (abbas.kouzani@newcastle.edu.au) or by phone 61-2-49216084. Both lecturers can also be contacted by appointment when teaching at PSB.

This course is also supported by a number of local tutors (information provided separately).

**TEXTBOOKS**
There is no recommended text book as such. The lecture notes we make available to you will cover all the material you need to know. For additional reading, we recommend the following texts:


**ASSESSMENT**

<table>
<thead>
<tr>
<th>PART A:</th>
<th>Quiz 1</th>
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<tbody>
<tr>
<td></td>
<td>Quiz 2</td>
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<tr>
<td></td>
<td>Lab 1</td>
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<td>Lab 2</td>
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<tr>
<td>PART B:</td>
<td>Quiz 3</td>
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<td>Lab 3</td>
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<td>Lab 4</td>
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<tr>
<td>FINAL EXAM</td>
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**Total: 100%**
PART-A TIMETABLE (Tentative)

6/11 Sunday
9:00 - 9:30 Introduction
9:30-10:30 Review of Basic Circuit Theory
10:30-11:30 Background Knowledge Test
  (Not counted towards final mark)
11:30-12:00 Solutions to Background Knowledge Test
12:00 - 1:00 Lunch Break
1:00 - 3:00 Dependent Sources
3:00 - 3:30 Exercise Problems
3:30 - 4:30 Matrix Algebra

7/11 Monday
7:00 - 7:30 Revision
7:30 - 9:30 DC Circuits: Nodal Analysis
9:30-10:00 Exercise Problems

9/11 Wednesday
7:00 - 7:30 Revision
7:30 - 9:30 DC Circuits: Mesh & Loop Analysis
9:30-10:00 Exercise Problems

11/11 Friday
7:00 - 7:30 Revision
7:30 - 9:30 Single-phase AC Circuits
9:30-10:00 Exercise Problems

13/11 Sunday
9:00 - 9:30 Revision
9:30-10:00 Frequency Response
10:00-11:00 Passive Filters
11:00-12:00 Quiz 1
12:00 - 1:00 Lunch Break
1:00 - 2:00 Resonance Circuits
2:00 - 2:30 Exercise Problems
2:30 - 4:30 3-phase AC Circuits

14/11 Monday
7:00 - 7:30 Solution to Quiz 1
7:30 - 8:00 Revision
8:00 - 9:30 Introduction to Operational Amplifiers (Op-Amp)
9:30-10:00 Exercise Problems

16/11 Wednesday
7:00 - 7:30 Revision
7:30 - 9:30 Op-Amp Circuits
9:30-10:00 Exercise Problems

18/11 Friday
7:00 - 9:00 Tutorial

21/11 Monday
7:00 - 8:00 Quiz 2
8:00 - 8:30 Solution to Quiz 2
8:30 - 9:00 Introduction to Lab Experiments

24/11 Thursday or 25/11 Friday
7:00 - 10:00 Lab 1: RLC Circuit Design  (Report due in Lab 2)

29/11 Tuesday or 30/11 Wednesday
7:00-10:00 Op-Amp Circuit Design  (Report due by 9:00am, 4/12
Sunday when Part B lectures start)
PART-B TIMETABLE (Tentative)

4/12 Sunday
9:00 - 9:30 Introduction
9:30-10:00 Background Knowledge Test
   (Not counted towards final mark)
10:00-11:30 Programmable logic devices
11:30-12:00 Solutions to Background Knowledge Test
12:00 -1:00 Lunch Break
1:00 - 2:30 VHDL basics
2:30 - 3:00 Break
3:00 - 4:30 Combinational Logic and VHDL
4:30 - 5:30 Exercise Problems

5/12 Monday
7:00 - 8:00 Tutorial: Getting started with Quartus II and VHDL Programming for Group 1
8:30 - 9:30 Tutorial: Getting started with Quartus II and VHDL Programming for Group 2

7/12 Wednesday
7:00 - 8:00 Sequential Logic and VHDL
8:00 - 9:30 Finite State Machines and VHDL
9:30-10:00 Exercise Problems

9/12 Friday
7:00 - 8:00 Computer Organisation
9:00 - 9:30 Introduction to the 8051 Microcontroller
9:30-10:00 Exercise Problems

11/12 Sunday
9:00 - 11:00 Assembly Language Programming 1
11:00-12:00 Quiz 3
12:00 - 1:00 Lunch Break
1:00 - 3:00 Assembly Language Programming 2
3:00 - 3:30 Break
3:30 - 4:30 Exercise Problems
4:30 - 5:30 Memory, interrupt, and peripherals

12/12 Monday
7:00 - 8:30 Memory, interrupt, and peripherals
8:30 - 9:00 Revision & Examination Overview
9:00 - 9:30 Solution to Quiz 3
9:30-10:00 Exercise Problems

14/12 Wednesday
7:00 - 8:00 Tutorial: Getting started with the 8051 simulator and assembly programming for Group 2
8:30 - 9:30 Tutorial: Getting started with the 8051 simulator and assembly programming for Group 1
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<thead>
<tr>
<th>Date</th>
<th>Time</th>
<th>Event Description</th>
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<tbody>
<tr>
<td>15/12 Thursday</td>
<td>7:00 - 7:30</td>
<td>Introduction to Lab3 for Group 1</td>
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<tr>
<td>16/12 Friday</td>
<td>7:30 - 10:00</td>
<td>Lab3: VHDL programming for Group 1</td>
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<td>17/12 Sunday</td>
<td>9:00 - 11:30</td>
<td>Lab3: VHDL programming for Group 1</td>
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<td>1:00 - 3:30</td>
<td>Lab3: VHDL programming for Group 2</td>
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<td>20/12 Tuesday</td>
<td>7:00 - 7:30</td>
<td>Introduction to Lab4 for Group 2</td>
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<td>7:30 - 10:00</td>
<td>Lab4: Assembly programming for Group 2</td>
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<tr>
<td>21/12 Wednesday</td>
<td>7:00 - 7:30</td>
<td>Introduction to Lab4 for Group 1</td>
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<td>7:30 - 10:00</td>
<td>Lab4: Assembly programming for Group 1</td>
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<td>22/12 Thursday</td>
<td>7:00 - 9:30</td>
<td>Lab4: Assembly programming for Group 2</td>
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<tr>
<td>23/12 Friday</td>
<td>7:00 - 9:30</td>
<td>Lab4: Assembly programming for Group 1</td>
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<td>27/12 Tuesday</td>
<td>7:00 - 9:00</td>
<td>Tutorial related to Part B for all students</td>
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<tr>
<td>28/12 Wednesday</td>
<td>7:00 - 9:00</td>
<td>Helpdesk for all students</td>
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**FINAL EXAM**

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<th>Time</th>
<th>Event Description</th>
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<tbody>
<tr>
<td>29/12 Thursday</td>
<td>7:00 - 10:10</td>
<td><strong>Final exam</strong> (10 minutes reading time+3 hours writing time)</td>
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